IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

VERVAIN, LLC,
            Plaintiff,
 	
      v.
 	
MICRON TECHNOLOGY, INC., et al.,
            Defendants.
	6:21-cv-00487-ADA

**MEMORANDUM OPINION AND ORDER GRANTING
DEFENDANTS' MOTION TO DISMISS UNDER RULE 12(b)(6) [ECF No. 17]**

Came on for consideration this date is Defendants' Motion to Dismiss Under Rule 12(b)(6). ECF No. 17 (the "Motion"), filed July 9, 2021, which argues that Plaintiff Vervain, LLC ("Vervain") failed to state a claim for patent infringement. Vervain responded on July 30, 2021, ECF No. 21, to which Defendants Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC (collectively, "Micron") replied on August 13, 2021, ECF No. 22.

I. BACKGROUND

Vervain filed this Action against Micron on May 10, 2021, asserting infringement of four patents: U.S. Patent Nos. 8,891,298 (the "'298 patent"), 9,196,385 (the "'385 patent"), 9,997,240 (the "'240 patent"), and 10,950,300 (the "'300 patent") (collectively, the "Asserted Patents"). ECF No. 1 (the "Complaint"). These patents generally relate to NAND flash memory that includes "a combination of single-level cell (SLC) and multi-level cell (MLC) NAND flash storage." '298 patent at 1:25–33. As the patents explain, "In SLC NAND flash technology, each cell can exist in one of two states, storing one bit of information per cell. Most MLC NAND flash memory has four possible states per cell, so it can store two bits of information per cell." *Id.* at 1:61–67. "MLC NAND flash enjoys greater density than SLC NAND flash, at the cost of a decrease in access speed

1

and lifetime." *Id.* at 3:19–21. But the Asserted Patents, which share a common specification, describe how "newer" memory systems employ MLC NAND, SLC NAND, and hard-disk drive solutions in one:
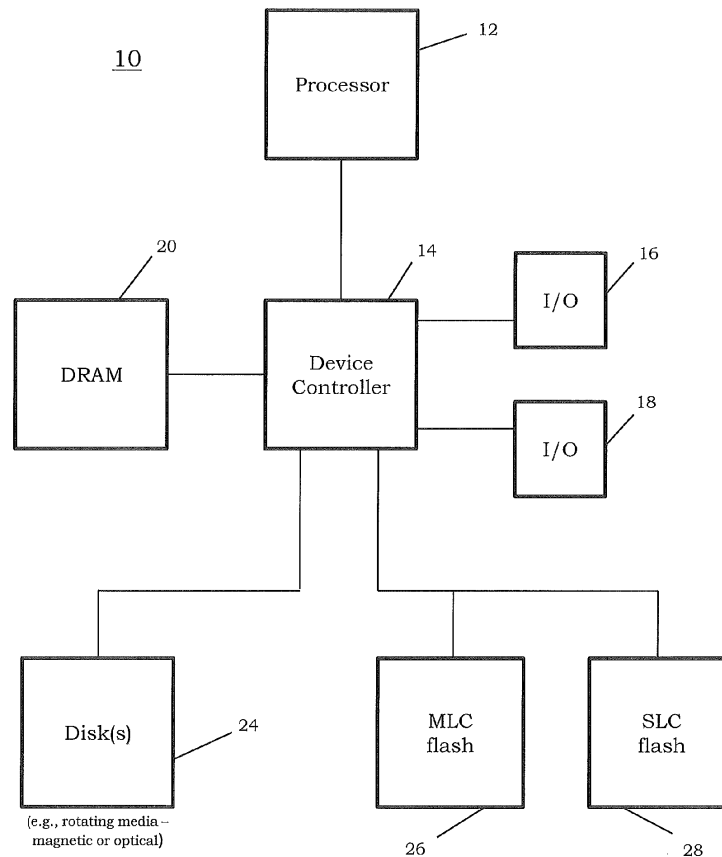

FIG. 1

See id. at 3:14–15, 4:64–5:15; *id.* at FIG. 1. According to Vervain, "The Asserted Patents are directed to specific techniques for efficiently using SLCs and MLCs to improve the overall performance of the flash memory." ECF No. 21 at 3.

The Complaint accuses solid-state drives ("SSDs") made, used, and/or sold by Micron of infringing the Asserted Patents. It specifically identifies Micron's M600 SATA SSD (the "M600" or "Accused Product(s)"), which it maps to the Asserted Patents' claims. *See* ECF No. 1 ¶¶ 59–

2

109. Micron has moved to dismiss that Complaint under Federal Rule of Civil Procedure 12(b)(6).

That Motion is now ripe for judgment.

II. LEGAL STANDARD

In patent cases, issues that are unique to patent law are governed by Federal Circuit law. *See Woods v. DeAngelo Marine Exhaust, Inc.*, 692 F.3d 1272, 1279 (Fed. Cir. 2012). But because motions to dismiss under Rule 12(b)(6) raise purely procedural issues, in patent cases, courts apply the law of the regional circuit—in this case, the Fifth Circuit—when deciding whether such a motion should be granted. *See In re Bill of Lading Transmission & Processing Sys. Patent Litig.*, 681 F.3d 1323, 1331 (Fed. Cir. 2012).

Rule 12(b)(6) requires that a complaint contain sufficient factual matter, if accepted as true, to "'state a claim to relief that is plausible on its face.'" *Ashcroft v. Iqbal*, 556 U.S. 662, 678 (2009) (quoting *Bell Atl. Corp. v. Twombly*, 550 U.S. 544, 570 (2007)). To meet this factual plausibility standard, the plaintiff must plead "factual content that allows the court to draw the reasonable inference that the defendant is liable for the misconduct alleged," based on "more than a sheer possibility that a defendant has acted unlawfully." *Id*. "Threadbare recitals of the elements of a cause of action, supported mere conclusory statements, do not suffice." *Id*. In resolving a motion to dismiss for failure to state a claim, the question is "not whether [the plaintiff] will ultimately prevail, . . . but whether [the] complaint was sufficient to cross the federal court's threshold." *Skinner v. Switzer*, 562 U.S. 521, 530 (2011). "The court's task is to determine whether the plaintiff has stated a legally cognizable claim that is plausible, not to evaluate the plaintiff's likelihood of success." *Lone Star Fund V (U.S.), L.P. v. Barclays Bank PLC*, 594 F.3d 383, 387 (5th Cir. 2010) (citing *Iqbal*, 556 U.S. at 678).

The U.S. Court of Appeals for the Federal Circuit's latest guidance on pleading standards for direct infringement comes from *Bot M8 LLC v. Sony Corporation of America*, 4 F.4th 1342

(Fed. Cir. 2021). The *Bot M8* Court affirmed-in-part and reversed-in-part an order dismissing direct infringement claims on four patents for failure to sufficiently plead. *See id.* at 1358. Critically, the opinion denounced a "blanket element-by element pleading standard for patent infringement," favoring instead a flexible inquiry into "whether the factual allegations in the complaint are sufficient to show that the plaintiff has a plausible claim for relief." *Id.* at 1352. The level of detail required to meet that standard depends on multiple factors, not limited to "the complexity of the technology, the materiality of any given element to practicing the asserted claim(s), and the nature of the allegedly infringing device." *Id.* at 1353. Under any standard, however, the complaint must support its entitlement to relief with "factual content," not just conclusory allegations that the accused product(s) meet every claim limitation. *Id.*

Under this clarified standard, the *Bot M8* Court reversed the dismissal of two direct infringement claims but affirmed the dismissal of two others. *Id.* at 1358. The complaint-at-issue alleged that the accused product, a PlayStation 4 ("PS4"), included "a control device that executes a 'fault inspection program' and 'completes the execution of the fault inspection program before the game is started,'" as required by two of the asserted patents. *Id.* at 1355. The complaint alleged four times that the PS4's CPU executes a "fault inspection program" on startup that completes before a game is started. *See id.* at 1355–56. But more critically, it identified specific error messages that the PS4 displays when faults are detected. For example, one error code states: "Cannot start the PS4. Cannot access system storage." *Id.* at 1356. Another reports that "required information to start the application cannot be found." *Id.*

These allegations satisfied the Federal Circuit. The defendant argued that even if these error codes suggested that fault inspection began at startup, "they say nothing about whether it completes

4

execution before a game starts," as recited in the claims. *Id.* This, the Court held, demanded too much:

> Bot M8 need not "prove its case at the pleading stage." . . . The FAC plausibly alleges that the PS4 completes its execution of the fault inspection program before the game is started and supports those assertions with specific factual allegations. Nothing more is required.

Id. (quoting *Nalco Co. v. Chem-Mod, LLC*, 883 F.3d 1337, 1350 (Fed. Cir. 2018)).

The Court was less satisfied with infringement allegations for two other patents. One required "a board including a memory in which a game program . . . and an authentication program . . . are stored" separate from a "motherboard" (the "board limitation"). *See id.* at 1353. The plaintiff argued that its complaint provided pages and pages of evidence showing how the PS4 met every claim element, including allegations that three different components satisfied the board limitation. *See id.* The defendant argued that the complaint did not plead a correspondence between the board limitation and the three components the plaintiff identified. *Id.* at 1353–54. Rather, the complaint taught away from the board limitation by alleging that the PS4's motherboard stores the authentication program. *See id.*

The Federal Circuit agreed with the defendant, finding that the complaint's "kitchen sink" approach to pleading "reveal[ed] an inconsistency" fatal to its infringement case for that patent. *Id.* at 1354. Alleging that the authentication program resides on the PS4's motherboard rendered the plaintiff's "infringement claim not even possible, much less plausible." *Id.* The plaintiff succeeded in pleading itself out of court. *See id.* (citing *Nalco*, 883 F.3d at 1348–50).

Another asserted patent includes claims requiring storing "game information including a mutual authentication program" on the same memory (the "mutual authentication" limitation). *See id*. The plaintiff argued that its complaint identified four different components satisfying this limitation. *See id.* The Federal Circuit found these allegations conclusory. The complaint did not

offer factual allegations supporting a "plausible inference that the PS4 actually stores the gaming information and mutual authentication program together." *Id.* They merely "track[ed] the claim language." *Id.* The *Bot M8* Court, therefore, affirmed dismissal of these claims.

The *Bot M8* opinion issued on the heels of *Disc Disease Solutions Inc. v. VGH Solutions, Inc.*, in which the Federal Circuit held that a complaint sufficiently pleaded direct infringement of claims directed to a spinal brace by "specifically identif[ying] the three accused products—by name and by attaching photos of the product packaging as exhibits—and alleg[ing] that the accused products meet 'each and every element of at least one claim.'" 888 F.3d 1256, 1260 (Fed. Cir. 2018). The Court was satisfied that this provided the accused infringer sufficient notice because the case involved a simple technology and only four independent claims. *See id.*

Though *Bot M8* and *Disc Disease* were respectively decided under the laws of the U.S. Courts of Appeals for the Ninth and Eleventh Circuits, the Fifth Circuit's pleading standards are not materially distinct. These opinions, then, supply welcome guidance regarding pleading requirements for direct infringement.

III. ANALYSIS

Vervain fails to sufficiently plead direct infringement of the Asserted Patents under 35 U.S.C. § 271(a). Micron argues that the Complaint fails to sufficiently plead direct infringement of the '298, '385 and '240 patents as it lacks sufficient factual allegations to support a reasonable inference that the M600 practices the claimed "hot blocks" and "data integrity test" limitations. The Court agrees as to the hot blocks limitations. Micron also argues that the Complaint fails to sufficiently plead direct infringement of the '300 patent as it lacks sufficient factual allegations to support a reasonable inference that the M600 practices its own "data integrity test" limitation. The Court agrees. Accordingly, the Court will dismiss Vervain's Complaint without prejudice.

A.   The "Hot Blocks" Limitations

Micron argues that the Complaint fails to sufficiently plead that the Accused Products practice what it calls the "hot blocks" limitations. *See* ECF No. 17 at 6–8. These limitations describe a technique in which "the system keeps track of the number of writes to each block of memory and then moves blocks receiving the highest number of writes from an MLC module to an SLC module." *Id.* at 2 (citing '298 patent at 6:24–35). According to Micron, claim 1 of the '298 patent captures this technique in the bolded limitations below:

> 1. A system for storing data comprising:
>
> at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;
>
> at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and
>
> a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to:
>
> a) maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;
>
> b) determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;
>
> **c) determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed; and**

> **d) allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module.**

'298 patent at 7:8–8:9 (emphasis added). [1] Micron asserts that the '385 and '240 patents recite similar limitations capturing this "hot blocks" technique. *See* ECF No. 17 at 3–4, 6–7; '385 patent at 7:36–8:4 (claim 1(c)–(d)); '240 patent at 8:36–41 (claim 6).

The Complaint alleges that the M600 uses a "wear-leveling" process practicing the hot blocks limitation. ECF No. ¶ 66. Micron disagrees. The Wear-Leveling Technical Note attached to the Complaint as Exhibit Z describes wear leveling as "a process by which a memory module allocates data writes to memory blocks that have previously been written to the fewest number of times." ECF No. 17 at 7 (citing ECF No. 1-26 (the "WL Note") at 2, 7). According to Micron, the claims require "writing data to the most durable type of memory," and wear leveling "merely involves writing data to whichever blocks have been written to the least." *Id.* "The WL Note makes clear," in Micron's judgment, "that wear leveling is entirely agnostic as to the type of memory . . . in which a data block is stored." *Id.*

Vervain's opposition remarks how the WL Note "never says wear leveling does not write from MLC blocks to SLC blocks." ECF No. 21 at 17. This argument, Micron retorts, shifts Vervain's burden to Micron, requiring Micron to disprove infringement at the dismissal stage. ECF No. 22 at 2.

Vervain also notes how Micron's Motion omitted reference to Exhibits R and V of the Complaint, which discuss the M600's use of a Dynamic Write Acceleration ("DWA") technique.

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[1] Micron presumably refers to the bolded limitations with the term "hot blocks"—a term Vervain takes umbrage with, ECF No. 21 at 4—because the '298 patent's specification refers to "blocks that receive frequent writes," like those described in step (d) of claim 1, as "hot" blocks. '298 patent at 6:24–29.

ECF No. 21 at 17–18. These exhibits purportedly acknowledge how writing to SLCs is faster and more efficient than writing to MLCs. ECF No. 21 at 8. Vervain supposes, then, that because DWA means to improve performance of the SSD, DWA is used in conjunction with wear leveling, and "data in the MLC blocks will presumably be rewritten to blocks of SLCs." *Id.* at 8, 17. Micron characterizes this reasoning as speculative. ECF No. 22 at 3. And it further contends that Vervain's opposition attempts to rewrite the Complaint. Specifically, the Complaint never cited to or relied on Exhibits R and V to allege that the Asserted Products practice the hot blocks limitations. *Id.* at 3. Micron also remarks how Exhibits R and V only mention SLC-to-MLC migration—not MLC-to-SLC migration, as required by the hot blocks limitations. *See id.* This, Micron argues, constitutes a teaching away. *See id.*

The Court holds that the Complaint has not sufficiently pleaded infringement of the '298, '385, and '240 patents' claims, having failed to plausibly allege infringement of the hot blocks limitations. The level of detail provided in Vervain's allegations did not meet the standard here, where the technology is not simple and the limitations-at-issue are material. The degree of detail required to sufficiently plead direct infringement depends on "the complexity of the technology, the materiality of any given element to practicing the asserted claim(s), and the nature of the allegedly infringing device." *Bot M8*, 4 F.4th at 1353. The technology-at-issue here is no less complex than that in *Bot M8*. And it is more complex than a spinal brace reciting primarily mechanical components, an invention the Federal Circuit deemed "simple." *Disc Disease*, 888 F.3d at 1260. The claims relate to software and firmware for using solid-state memory—they concern intangible instructions for managing data acting on hardware. *Cf. Fractus v. TCL Corp.*, No. 2:20-CV-00097-JRG, 2021 U.S. Dist. LEXIS 114011, at *9 (E.D. Tex. June 2, 2021) (suggesting software-based claims may demand a higher level of pleading).

The Court finds that the hot block limitations are material to practicing the asserted claim, at least because the relevant prosecution history and the Complaint suggest that these limitations capture the point of novelty. The *Bot M8* opinion does not elaborate on what "the materiality of any given element to practicing the asserted claim(s)" means. In the context of literal infringement, every claim element is material. *See V-Formation, Inc. v. Benetton Grp. SpA*, 401 F.3d 1307, 1312 (Fed. Cir. 2005) ("Literal infringement requires that each and every limitation set forth in a claim appear in an accused product."). It is unclear, then, how the *Bot M8* Court intended for district courts to categorize elements by their "materiality." But, in this Court's judgment, a higher level of detail in pleading infringement may—depending on the complexity of the technology—be demanded for elements clearly "material" to novelty and non-obviousness. In cases involving complex technology, a complaint nakedly alleging that the accused product practices the claimed invention's point of novelty will rarely suffice. A plaintiff cannot establish "why it is plausible that the accused product infringes the patent claim," *Bot M8*, 4 F.4th at 1353, by merely articulating why it is plausible that the accused product practices the prior art. Pleading only the latter begs the "obvious alternative explanation" that the accused infringer is merely practicing the prior art. *Twombly*, 550 U.S. at 567.

The hot blocks limitations lay at the point of novelty, and so this Court will demand a higher level of pleading. The Court takes judicial notice of the prosecution history of the '298 patent.[2] In his September 2, 2014, Notice of Allowance, the patent examiner noted: "The prior art

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[2] Courts may take judicial notice of government records, like prosecution history available on the U.S. Patent & Trademark Office's Public PAIR site, even when resolving a Rule 12(b)(6) motion. *See Lovelace v. Software Spectrum*, 78 F.3d 1015, 1017 (5th Cir. 1996); *Jenny Yoo Collection, inc. v. Watters Designs, Inc.*, Civil Action No. 3:17-cv-3197-M, 2018 U.S. Dist. LEXIS 114623, at *19 n.8 (N.D. Tex. June 6, 2018); *Integrated Tech. Sys. v. First Internet Bank of Ind.*, No. 2:16-CV-00417-JRG-RSP, 2017 U.S. Dist. LEXIS 21309, at *4 (E.D. Tex. Jan. 30, 2017).

of record fails to teach that the controller allocates those blocks that receive the most frequent

writes by transferring the respective contents of those blocks to the at least one SLC non-volatile

memory."[3] Indeed, the applicant amended steps (c) and (d) into claim 1 to overcome the prior art

and reach allowance by the next office action.[4] Even the Complaint seems to describe the hot

blocks limitations as being the nut of the invention. *See* ECF No. 1 ¶ 43. Based on the complexity

and materiality of the claims, the Court concludes that pleading infringement of the '298, '385,

and '240 patents' claims will require more than attaching photos of the Accused Products and

summarily alleging that each and every limitation is satisfied. *But see Disc Disease*, 888 F.3d at

1260; ECF No. 21 at 15 (citing other cases in that vein, which this Court finds inapposite).

Attaching photos of the M600 or its packaging would do little good here where the claims are

primarily directed to firmware operating upon nanometers-wide cells (typically described in the

abstract).

The Complaint maps the hot blocks limitations to the M600 at paragraphs 65 and 66. As

noted above, these paragraphs allege that the M600 "employs wear leveling techniques that

employ block erase counting." ECF No. 1 ¶ 65. In support, the Complaint cites to the WL Note,

which describes two wear-leveling methods. *Id.* ¶ 65 & n.27. But neither technique can be

stretched to establish a reasonable inference that the M600 performs the hot blocks limitations

(under any reasonable construction of the relevant terms). The first technique, dynamic wear

leveling, selects free blocks with the lowest erase count for the next write. ECF No. 1-26 at 3. This

technique does not suggest transferring contents from one block to another. Accordingly, the

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[3] Notice of Allowance, Prosecution History of U.S. Patent Application No. 13/455,267 (Sept. 2, 2014).

[4] *See* Amendment, Prosecution History of U.S. Patent Application No. 13/455,267 (Aug. 19, 2014).

M600's employment of dynamic wear leveling does not lead to a reasonable inference that the M600 transfers contents of the most frequently written-to blocks to some other block (let alone to SLC non-volatile memory), as required by claim 1.

The second wear leveling method is static wear leveling, in which "Blocks that contain static data with erase counts that begin to lag behind other blocks will be included in the wear-leveling block pool, with the static data being moved to blocks with higher erase counts." ECF No. 1-26 at 4. This, at least, is an improvement upon dynamic wear leveling, insofar as it discloses migrating contents from one block to another. It is still not enough. Claim 1 of the '298 patent requires that contents are transferred out of the most active blocks—blocks receiving the most frequent writes. Static wear leveling describes the opposite phenomenon: contents are transferred out of the least active blocks to the most active blocks. The WL Note does not suggest that migration occurs in the other direction. Accordingly, the M600's employment of static wear leveling does not lead to a reasonable inference that the M600 transfers contents of the most frequently written-to blocks to some other block (let alone to SLC non-volatile memory), as required by claim 1.

The WL Note's description of these two wear-leveling techniques is consistent with the '298 patent's own description, in the "BACKGROUND OF THE DISLOSURE" section, of the same two wear-leveling techniques. *See* '298 patent at 3:1–13. Micron's Motion noted this consistency, *see* ECF No. 17 at 7, and Vervain offered no response. In this context, the Court refuses to find that Micron's practicing techniques the Asserted Patents characterize as conventional—wear leveling—leads to a reasonable inference that Micron practices the presumably novel invention claimed in these three Asserted Patents.

The Vervain opposition's reliance on Exhibits R and V is unavailing. Vervain emphasizes the number of exhibits it relied on to "provide the factual basis for its infringement allegations." ECF No. 21 at 6–7. But "it is the *quality* of the allegations, not the *quantity*, that matters." *Bot M8*, 4 F.4th at 1353. The Complaint cites Exhibit R in support of the contention that the M600 includes a system for storing data. ECF No. 1 ¶ 59 & n.19. It cites Exhibit V in support of the contention that the M600 includes one "SLC non-volatile memory module comprising a plurality of individually erasable blocks." *Id.* ¶ 61 & n.23. These exhibits are not, under any reasonable reading, cited in support of mapping the M600 to the hot blocks limitations. Vervain cannot rehabilitate its Complaint through its opposition. *See Energy Coal v. CITGO Petroleum Corp.*, 836 F.3d 457, 462 n.4 (5th Cir. 2016) ("The complaint may not be amended by the briefs in opposition to a motion to dismiss."). Vervain posits that the Complaint put Micron on "notice of what activity . . . is being accused of infringement," *K-Tech Telecomms., Inc. v. Time Warner Cable, Inc.*, 714 F.3d 1277, 1284 (Fed. Cir. 2013)—Micron merely had to review every exhibit to the Complaint, regardless of where cited, and combine the correct subset of them to conjure the particular mapping prescribed in Vervain's opposition. This goes too far. The Court disregards Vervain's arguments as to Exhibits R and V, offered for the first time in opposition to Micron's Motion. (Even if they were considered, the Court is not persuaded that Vervain has adequately explained how DWA cures the specific faults, identified above, related to the wear-leveling allegations.)

To be sure, Vervain "need not prove its case at the pleading stage." *Nalco*, 883 F.3d at 1350. And Vervain should be commended for providing an element-by-element mapping. But a direct infringement claim is not sufficiently pleaded so long as plaintiff provides a claim chart or element-by-element mapping. The Court must consider whether the factual allegations therein,

"when taken as true, articulate why it is plausible that the accused product infringes the patent claim." *Bot M8*, 4 F.4th at 1353; *see also id.* ("[I]t is the *quality* of the allegations, not the *quantity*, that matters."); *Metricolor LLC v. L'Oreal S.A.*, 791 F. App'x 183, 188 (Fed. Cir. 2019) (rejecting the complaint's allegation that the accused product included an "air-tight reclosing seal" after finding no such seal on the product). The Complaint fails to do that, even when allegations describing the M600's use of wear leveling are taken as true. The Complaint's only other allegations regarding the hot blocks limitations "merely track the claim language" and are therefore insufficient to give rise to a reasonable inference that the M600 practices the claims. *Id.* at 1355; *Chhim v. UT-Austin*, 836 F.3d 467, 469 (5th Cir. 2016) ("[W]e do not credit conclusory allegations or allegations that merely restate the legal elements of a claim."). The facts alleged simply fail, in this Court's judgment, to "articulate why it is plausible that the accused product infringes the patent claim." *Id.* at 1354.

B.   The "Data Integrity Test" Limitations of the '298, '385, and '240 Patents

Each of the asserted claims of the '298, '385, and '240 patents also require a "data integrity test." Micron proposes step (c) from claim 1 of the '298 patent as a representative limitation:

> . . . wherein the controller is adapted to . . . b) determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module . . . .

'298 patent at 7:26–33. According to the Complaint, it is plausible that the M600 practices this limitation because it "incorporates defect and error management technology." ECF No. 1 ¶ 64. The Complaint continues, "[t]he controller addresses data integrity issues by remapping data," citing in support Exhibit Y, Micron's Technical Note on COPYBACK Operations. *Id.* ¶ 64 & n.27 (citing ECF No. 1-25 (the "COPYBACK Note")).

In Micron's view, this is insufficient. It argues that the COPYBACK Note describes how "if data errors were detected, those errors would be corrected by the controller *before* that data was written." ECF No. 17 at 9 (citing ECF No. 1-25 at 2). "And the detection of an error would not affect the location to which the data was being written, let alone cause the data to be written to an SLC module." *Id.* In response, Vervain again argues—as it did in the context of the hot blocks limitations—that Micron's Motion ignores DWA as described in Exhibits R and V. ECF No. 21 at 18. This Court disposes of that argument as it did above. *See supra* Section III.A. Vervain further responds that the COPYBACK Note "never says data is not written to SLCs." ECF No. 21 at 18. This representation may suffice to show that Vervain has not pleaded itself out of court; it does not establish that Vervain has otherwise sufficiently pleaded infringement.

Micron's arguments—as to error-correction timing and whether error detection must "affect" the location to which data is written—draw too-thin distinctions better suited to resolution at a later stage, after the claims have been construed. *See Nalco*, 883 F.3d at 1350.

C.   The "Data Integrity Test" Limitations of the '300 Patent

The '300 patent's claims also recite a "data integrity test" limitation, bolded in the reproduction of claim 1 below:

> 1. A system for storing data comprising:
>
> memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space;
>
> at least one controller to operate memory elements and associated memory space;
>
> at least one MLC nonvolatile memory element that can be mapped into the MLC memory space;
>
> at least one SLC nonvolatile memory element that can be mapped into the SLC memory space;

15

at least one random access volatile memory;

an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and random access volatile memory;

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory;

the controller performing a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation performed thereon by comparing the stored data to the retained data in the random access volatile memory;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

’300 patent at 7:37–8:12 (emphasis added); *see also* ECF No. 17 at 4–5. The Complaint states that

the M600 “performs a data integrity test by comparing data stored in the flash memory with data

retained in the DRAM,” citing a Micron document describing data path protection. ECF No. 1

¶ 108 (citing ECF No. 1-23 (“Protection Brief”) at 1, 3). According to Micron’s Motion, the

Protection Brief describes a “parity check,” involving comparing an embedded logical address to

a corresponding address stored in a logical-to-physical address. ECF No. 17 at 10. This, the Motion

contends, is not a “data integrity test.” *Id.* Micron also alleges that the Complaint fails to allege

“that a test failure results in the user data being transferred to a different physical address.” *Id.*

Vervain responds, noting that the Protection Brief "never states that a data transfer does not occur." ECF No. 21 at 18. Again, this representation may suffice to show that Vervain has not pleaded itself out of court, but it does not establish that Vervain has otherwise sufficiently pleaded infringement. Vervain also contends that "Micron never mentions Exhibits R, X, and Y," yet never explains *how* these exhibits address Micron's arguments. *Id.* Finally, Vervain argues that "Defect and Error Management involves 'bad block management' and rewriting bad blocks to other locations," citing to another Technical Note on wear leveling. *Id.* (citing ECF No. 1-23 (the "Second WL Note") at 5). The Second WL Note states that "it is recommended that you implement garbage collection and bad block management algorithms." ECF No. 1-23 at 5. It does not allude to what "bad block management algorithms" are and Vervain does not deign to explain how these algorithms relate to the parity check described in the Protection Brief. Yet Vervain proclaims that these "bad blocks" are "blocks that have failed a data integrity test, and the failed data integrity test 'result in' the 'bad blocks' being rewriting to new locations." ECF No. 21 at 18.

The Court is unconvinced by Vervain's opposition and concludes that the Complaint has not sufficiently pleaded infringement of the '300 patent's claims. Vervain is required to plead infringement of these data integrity test limitations with more specificity than it mustered. These limitations were, after all, critical to issuance of these claims. The prosecution history reflects how these limitations permitted the claims of the '300 patent to pass to allowance.[5] And the Complaint, again, notes how these limitations reflect a critical part of the invention. *See* ECF No. 1 at 43.

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[5] Amendment, Prosecution History of U.S. Patent Application No. 16/066,299 (Oct. 8, 2020) (amending in the "comparing" limitations); Notice of Allowance, Prosecution History of U.S. Patent Application No. 16/066,299 (Jan. 27, 2021) (distinguishing closest prior art based on "remapping" limitations).

Despite the importance of this limitation, Vervain falls short, though only just, of adequately pleading that the M600 practices this limitation. The Court is willing to find that Vervain sufficiently pleaded how the M600 "perform[s] a data integrity test" based on allegations directed to the Protection Brief's description of a parity check. *See* ECF No. 1 ¶ 108. The Court is also willing to find that Vervain has sufficiently pleaded how the M600 "remap[s] the address space to a different physical range of addresses," based on, for example, citation to the COPYBACK Note or even the Second WL Note. *See id.* ¶ 110; ECF No. 21 at 19; *see also supra* Section III.B. The Court agrees with Vervain that Micron's issues with these specific elements are best addressed during or after claim construction. *See Nalco*, 883 F.3d at 1350. But, even considering all allegations in a light most favorable to Vervain, the Complaint does not plead a logical connection between the alleged mapping and a failure of the alleged "data integrity test," let alone that the former is the result of the latter, as required by the claims.

To its credit, the Complaint states that "[t]he controller addresses data integrity issues by remapping data," citing the COPYBACK Note. ECF No. 1 ¶ 110. But the Complaint does not allege that the data integrity issues addressed in the COPYBACK Note are comparable, analogous, or in any way relevant to the data integrity issues addressed in the Protection Brief. The COPYBACK Note describes checking for whether data being transferred within NAND memory has been corrupted, and how to correct that error. *See* ECF No. 1-25 at 1. The Protection Brief describes a parity check ensuring that the SSD receives data from the logical address it intended to request data from. *See* ECF No. 1-23 at 3. These are two disparate types of errors. The Complaint does not suggest why the COPYBACK Note's alleged "remapping" would be used to correct the error described in the Protection Brief. It is not enough to point to accused elements; Vervain must "offer factual allegations that support a plausible inference" that those elements perform the

18

relevant limitations. 4 F.4th at 1355. It has not done. Accordingly, Vervain has not raised its right

to relief "above the speculative level." *Twombly*, 550 U.S. at 555.

IV. CONCLUSION

For the foregoing reasons, the Court **GRANTS** Micron's Rule 12(b)(6) Motion to Dismiss

Vervain's direct infringement claims. It is therefore **ORDERED** that all Vervain's claims against

Micron are **DISMISSED** without prejudice. Having ordered dismissal without prejudice, the

Court **GRANTS** leave for Vervain to file an amended complaint within 14 days hereof. Failure of

Vervain to file an amended complaint within the next 14 days shall be construed by the Court as

an election by Vervain not to re-urge its complaint in this case, and in such event the Clerk shall

close this case.

SIGNED this 3rd day of January, 2022.

ALAN D ALBRIGHT
UNITED STATES DISTRICT JUDGE